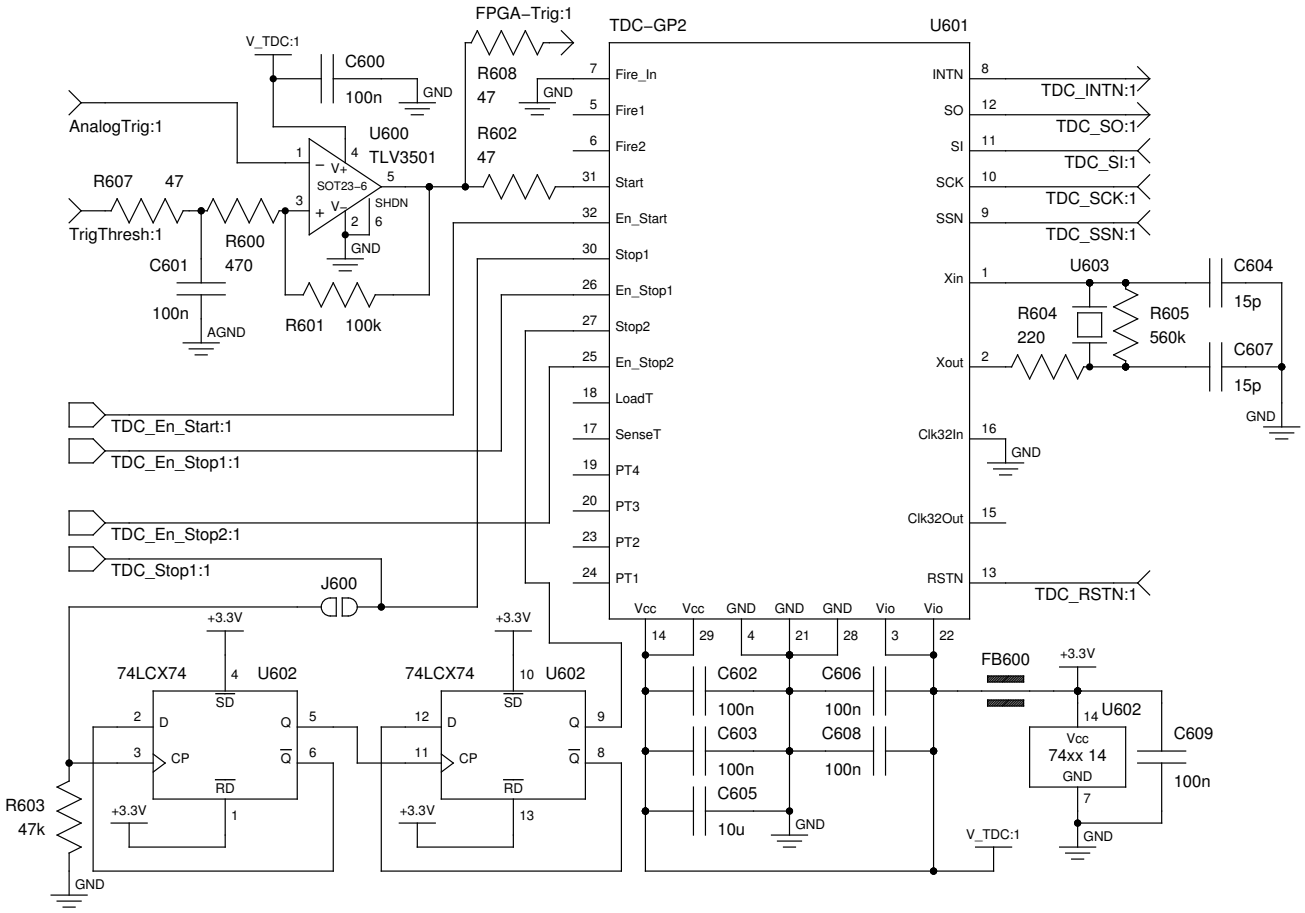
Analog Trigger and TDC (Time to Digital Converter) for

Equivalent Time Sampling (ETS) also called

Random−Sampling or Postcorrelated Undersampling



Remarks

− Clock Prescaler (FF) should be obsolete

− En_Start/En_Stop from FPGA

− Stop from ADC Clock Out

DAD/DSO, Analog Trigger & TDC	
File: TDC.sch	Sheet: 6 of 19
Author: S. Salewski	Rev: A 0.13
Copyright: All Rights Reserved	Date: 06−SEP−2009