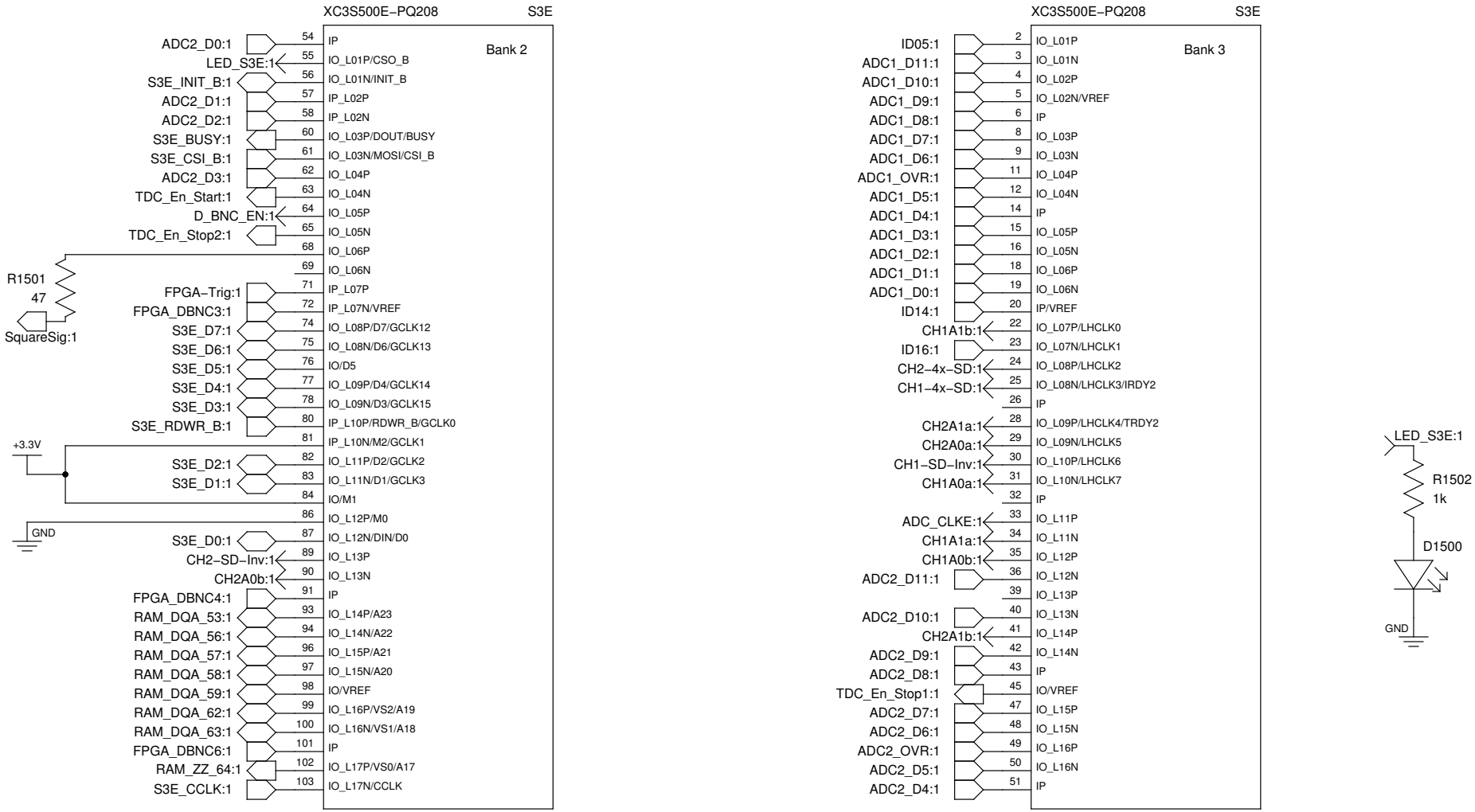

Remarks

− Signals with plain arrow symbol are low speed

− CCLK, BUSY, RDWR, CSI and D[7:0] is used for communication with uC after configuration too!

DAD/DSO, FPGA B2,B3	
FPGA_B2B3.sch	Sheet: 15 of 19
Author: S. Salewski	Rev: A 0.11
Copyright: All Rights Reserved	Date: 06−SEP−2009